Abstract

An arithmetic computation circuit is implemented to significantly increase throughput and thereby permit processing of relatively large binary numbers in a relatively small period

5   of time. In one embodiment, the arithmetic computation circuit adapted to add a first binary operand of N bits and a second binary operand of M bits, where N is greater than or equal to M. The circuit includes an adder and a multiplexer circuit. The adder is adapted to combine representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout. The multiplexer circuit is adapted

10   to output a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand; the selection of these inputs is responsive to selection data that is a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.